THE HONG KONG POLYTECHNIC UNIVERSITY
香港理工大學

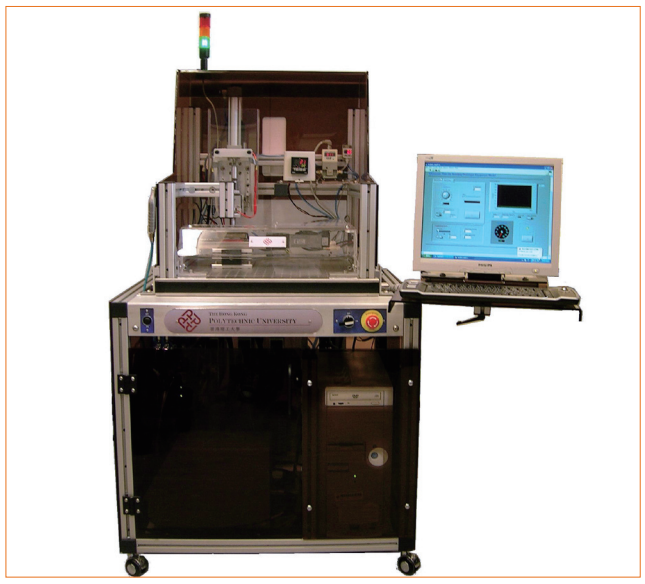
超薄半導體集成電路晶片管芯焊接超聲技術平台
Ultrasonic Semiconductor Thin-Die Bonding Platform

這項全新的技術平台包括獨特的超聲焊接裝置，可持續的自動化生產設備及具有室溫和高效的綠色製程

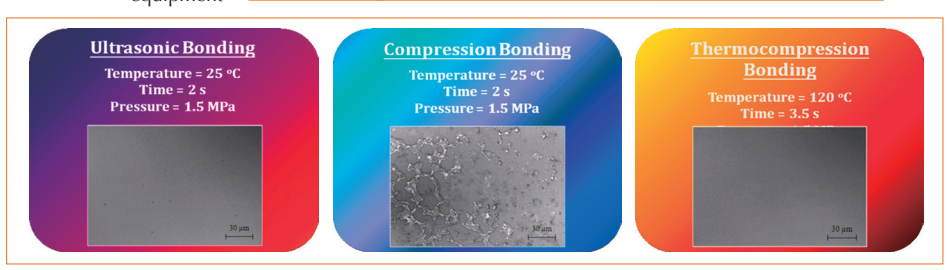
A novel ultrasonic technological platform comprising a critical ultrasonic bonding device, a sustainable automated manufacturing equipment, and a green process for room-temperature and rapid bonding of semiconductor thin-dies onto various substrates

專利編號：13/340,168 (美國), 8,129,220 (美國),
ZL201010262578.6 (中國), 099128156(台灣)

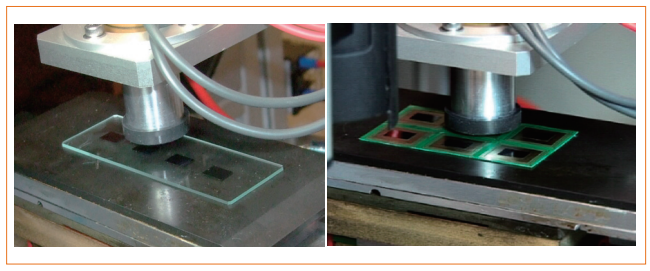
理大的研究小組通過精湛的科研技術，成功研發出一項用於超薄半導體集成電路晶片管芯焊接的超聲技術平台。這項全新的技術平台包括獨特的超聲焊接裝置，可持續的自動化生產設備及具有室溫和高效的綠色製程，可把超薄半導體集成電路晶片焊接於各種基板上。現時最先進的超薄半導體集成電路晶片管芯焊接設備及製程以熱壓技術為基礎，其本質受制於過高的製程溫度（攝氏120-160度）、較長的製程時間（3-10秒）、在一個製程週期內只可焊接單塊晶片、持續高溫加熱於已焊接及準備焊接的晶片及基板上、以及有限的可焊接基板種類。香港理工大學最新研發的超聲管芯焊接設備及製程，不僅具有獨特的室溫（攝氏25度）及高效（少於2秒）的焊接能力，並且安全、乾淨（環保）和可靠，同時能夠在單一的製程週期內在各種基板上堆疊焊接超過5層超薄半導體集成電路晶片。



理大研發的超聲管芯焊接設備
Ultrasonic semiconductor thin-die bonding equipment



超聲管芯焊接製程及質量(左)與氣壓管芯焊接製程及質量(中)及熱壓管芯焊接製程及質量(右)的比較
Process results of ultrasonic bonding (left), compression bonding (middle), and thermocompression bonding (right) of COG package



在室溫中應用超聲管芯焊接技術於超薄半導體集成電路晶片與玻璃接合(COG)之組件(左)及超薄半導體集成電路晶片與聚合物軟膜接合(COF)之組件(右)
Room-temperature ultrasonic bonding of COG package (left) and COF package (right)

PolyU's research team has developed a novel ultrasonic technological platform consisting of a critical ultrasonic bonding device, a sustainable automated manufacturing equipment, and a green process to enable room-temperature and rapid bonding of semiconductor thin-dies onto various substrates. State-of-the-art thermocompression thin-die bonding equipment and process suffer intrinsically from high process temperature (120-160 °C), long process time (3-10 s), single die bonding per process cycle, continual heating of fresh and post-bonded dies and substrates, and limited bondable substrates. PolyU's newly developed ultrasonic thin-die bonding equipment and process not only feature unique room-temperature (25 °C) and rapid (<2 s) bonding capabilities in a safe, clean (green), and reliable manner, but also enable simultaneous stacked die bonding in excess of five layers of thin-dies within a single bonding process cycle and for various substrates.

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特色與優點

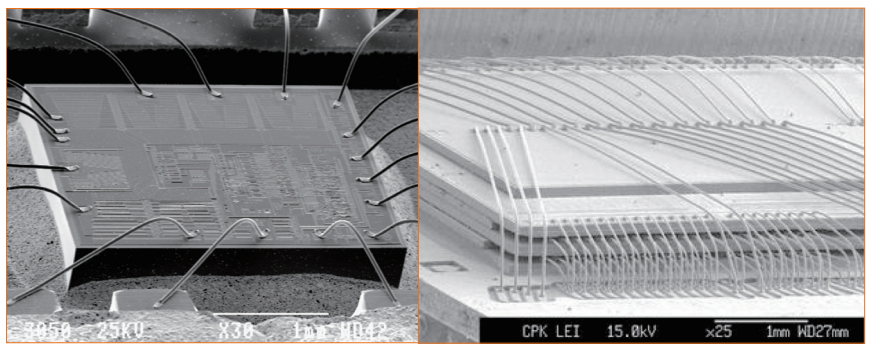
- 室溫製程（攝氏25度）
- 較短的製程時間（少於2秒）
- 在單一的製程週期內堆疊焊接超過5層超薄半導體集成電路晶片
- 可應用於各種基板 (例如：玻璃基板、印刷線路板、聚合物軟膜基板、金屬基板等）
- 避免持續高溫加熱於已焊接及準備焊接的晶片及基板上
- 安全、乾淨（環保）和可靠

應　用

- 半導體集成電路晶片管芯焊接：半導體封裝、半導體集成電路組件及其電子產品的關鍵製程之一，包括、但不限於晶片與玻璃接合（COG）之組件、晶片與線路板接合（COB）之組件及晶片與聚合物軟膜接合（COF）之組件
- 先進的堆疊式半導體集成電路晶片管芯焊接
- 各種電子組件之綠色組裝，包括、但不限於聚合物軟膜與玻璃接合（FOG）之組件及聚合物軟膜與線路板接合（FOB）之組件

獎　項

第三十七屆瑞士日內瓦國際發明及創新技術與產品展覽
- 金獎 (2009年4月)



先進的堆疊式超薄半導體集成電路晶片組件(共六層、每層厚度少於75微米)(左)與傳統的半導體集成電路晶片組件(單層、其厚度約500微米)(右)的比較
Stacked semiconductor thin-dies (6 layers in total, ≤75 μm thickness each) (left) vs. traditional single semiconductor die (single layer, ~500 μm thickness) (right)

Patent No: 13/340,168 (US), 8,129,220 (US),
ZL201010262578.6 (China), 099128156(Taiwan)

Special Features and Advantages

- Room-temperature process (25 °C)
- Short process time (<2 s)
- Stacked die bonding of multiple dies within a single bonding process cycle
- Applicable to various substrates (e.g., glass, PCB, flex, metal, etc.)
- Avoiding continual heating of fresh and post-bonded dies and substrates
- Safe, clean (green), and reliable

Applications

- Semiconductor die bonding – A critical process for the manufacturing of semiconductor packages, including, but not limited to, chip-on-glass (COG), chip-on-board (COB), and chip-on-flex (COF) packages
- Advanced stacked semiconductor die bonding
- Green assembly of various electronics modules, including, but not limited to, flex-on-glass (FOG) and flex-on-board (FOB) modules

Award

Gold Award - 37th International Exhibition of Inventions, New Techniques and Products, Geneva (April 2009)